CLAIMS

1. A method for determining a dominant logic state in an integrated circuit, comprising:

    using a representation of the integrated circuit to determine a first partition and a second partition wherein the first partition includes a first power supply node and the second partition includes a second power supply node;

    determining a partial logic state corresponding to the first and second partitions;

    modifying the representation according to the partial logic state; and

    using the modified representation to determine the dominant logic state.

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2. The method of claim 1, further comprising:

    determining a plurality of partition groups each having two partitions by iteratively moving at least one node from the second partition to the first partition;

    determining a partial logic state corresponding to each of the plurality of partition groups; and

    for each partial logic state, modifying the representation to determine at least one dominant logic state.

3. The method of claim 2, wherein the at least one node is not the second power supply node.

4. The method of claim 2, wherein modifying the representation includes at least one of removing edges and merging nodes according to known inputs of the partial logic state.

5. The method of claim 2, further comprising determining a first set of feasible inputs for each partial logic state, wherein:

if the first set is empty, enumerating states of the unknown inputs whose edges remain in the representation after modifying the representation to determine the at least one dominant logic state, and

if the first set is not empty, updating the partial logic states based on the feasible inputs.

6. The method of claim 5, further comprising:

if the first set is not empty, modifying the graph representation and determining a second set of feasible inputs after updating the partial logic states.

7. The method of claim 5, wherein enumerating is performed to determine a plurality of dominant logic states.

8. The method of claim 1, wherein the dominant logic state corresponds to a transistor within the integrated circuit that sees a drain-to-source voltage of the first power supply when the transistor is off.

9. The method of claim 1, wherein the representation is a graph representation

comprising nodes and edges.

10. The method of claim 9, wherein modifying the graph representation includes at least one of removing edges and merging nodes according to known inputs of the partial state.

11. The method of claim 1, wherein the integrated circuit is a DC-connected component (DCC).

12. A method for determining a leakage current of an integrated circuit, comprising:

partitioning the integrated circuit into at least one DC-connected component (DCC);

determining a dominant logic state corresponding to the at least one DCC; and

calculating a leakage current for the at least one DCC corresponding to the dominant logic state.

13. The method of claim 12, wherein determining is further characterized as determining a set of dominant logic states corresponding to the at least one DCC.

14. The method of claim 13, wherein calculating comprises calculating a leakage current corresponding to each dominant logic state within the set of dominant logic states.

15. The method of claim 12, wherein the DCC includes at least one input, the method further comprising:

determining a probability corresponding to the at least one input; and

using the probability and the leakage current to calculate an average DCC leakage current.

16. The method of claim 15, wherein the integrated circuit is partitioned into a plurality of DCCs, each DCC including at least one input, the method further comprising:

determining a set of dominant logic states corresponding to each of the plurality of DCCs;

calculating a leakage current corresponding to each dominant logic state within each set of dominant logic states;

determining a probability corresponding to the at least one input of each DCC;

using the corresponding probability and the corresponding leakage current to calculate an average DCC leakage current for each DCC; and

calculating an average circuit leakage for the integrated circuit using the average DCC leakage currents.

17. The method of claim 12, wherein the integrated circuit is partitioned into a plurality of DCCs, the method further comprising:

determining a set of dominant logic states corresponding to each of the plurality of DCCs;

calculating a leakage current corresponding to each dominant logic state

within each set of dominant logic states; and

calculating an average circuit leakage for the integrated circuit.

18. The method of claim 12, wherein:

the at least one DCC is coupled to a first power supply; and

the dominant logic state corresponds to a transistor within the DCC that sees a drain-to-source voltage of the first power supply when the transistor is off.

19. The method of claim 12, wherein determining the dominant logic state corresponding to the at least one DCC comprises:

using a representation of the DCC to determine a first partition and a second partition wherein the first partition includes a first power supply node and the second partition includes a second power supply node;

determining a partial logic state corresponding to the first and second partitions;

modifying the representation according to the partial logic state; and

using the modified representation to determine the dominant logic state.

20. The method of claim 12, wherein calculating the leakage current for the at least one DCC corresponding to the dominant logic state comprises:

constructing a graph having nodes and edges according to the dominant logic state of the integrated circuit;

calculating a leakage for each transistor in a first set of transistors;

modifying the graph based on the first set of transistors;

calculating a leakage for each transistor in a second set of transistors; and

calculating the leakage current for the at least one DCC using the leakages for the transistors in the first set of transistors and the leakages for the transistors in the second set of transistors.

21. A method of improving performance of an integrated circuit, comprising:

for each transistor of the integrated circuit having a first threshold voltage level, calculating a first value based at least in part on delay and leakage corresponding to a second threshold voltage level;

selecting one of the transistors of the integrated circuit based on the first values;

setting the selected one of the transistors to the second threshold voltage level; and

modifying an area of at least one transistor within the integrated circuit.

22. The method of claim 21, further comprising determining a cone of influence of the selected one of the transistors wherein the at least one transistor is within the cone of influence.

23. The method of claim 22, wherein the selected one of the transistors and the at least one transistor is a same transistor.

24. The method of claim 22, wherein modifying includes modifying an area of each transistor within the cone of influence.

25. The method of claim 21, further comprising:
sizing the integrated circuit to a predetermined area after modifying the area of the at least one transistor.

26. The method of claim 25, further comprising determining a cone of influence of the selected one of the transistors, wherein modifying includes modifying an area of each transistor within the cone of influence.

27. The method of claim 25, wherein the integrated circuit has a first area prior to calculating the first values and the predetermined area approximately equals the first area.

28. The method of claim 25, further comprising:
determining a circuit performance;
if the circuit performance is below a predetermined performance level, repeating calculating the first values, selecting one of the transistors, setting the selected one of the transistors, modifying the area of the at least one transistor, and sizing the integrated circuit.

29. The method of claim 21, further comprising:
determining a circuit performance;
if the circuit performance is below a predetermined performance level, repeating calculating the first values, selecting one of the transistors, setting the selected one of the transistors, and modifying the area of the at least one transistor.

30. The method of claim 21, wherein calculating the first value based at least in part on the delay and the leakage corresponding to the second threshold voltage level comprises:

partitioning the integrated circuit into at least one DC-connected component (DCC);

determining a dominant logic state corresponding to the at least one DCC; and

calculating a leakage current for the at least one DCC corresponding to the dominant logic state.

31. An improved integrated circuit manufactured using the method of claim 21.

32. A method for calculating a leakage current of an integrated circuit, comprising:

constructing a graph having nodes and edges according to a dominant logic state of the integrated circuit;

calculating a leakage for each transistor in a first set of transistors;

modifying the graph based on the first set of transistors; and

calculating a leakage for each transistor in a second set of transistors.

33. The method of claim 32, wherein the integrated circuit is a DC-connected component (DCC).

34. The method of claim 32, wherein constructing the graph comprises modifying the graph according to a dominant logic state of the integrated

circuit.

35. The method of claim 32, wherein the first set of transistors includes transistors of the integrated circuit that are off and are coupled to both a first power supply node and a ground node.

36. The method of claim 35, wherein calculating the leakage for each transistor in the first set of transistors is performed using a lookup table.

37. The method of claim 36, wherein calculating the leakage for each transistor in the second set of transistors comprises:

calculating a node voltage; and

using a lookup table.

38. The method of claim 32, wherein modifying the graph includes removing from the graph an edge corresponding to each of the transistors in the first set of transistors.

39. The method of claim 30, wherein the first set of transistors and the second set of transistors are mutually exclusive.

40. The method of claim 30, further comprising calculating a leakage current of the integrated circuit by summing the leakages for the transistors in the first set and the leakages for the transistors in the second set.

41. A computer readable medium, comprising:

a first plurality of instructions for receiving a representation of an integrated circuit;

a second plurality of instructions for determining a first partition and a second partition wherein the first partition includes a first power supply node and the second partition includes a second power supply node;

a third plurality of instructions for determining a partial logic state corresponding to the first and second partitions;

a fourth plurality of instructions for modifying the representation according to the partial logic state; and

a fifth plurality of instructions for using the modified representation to determine the dominant logic state.

42. A computer readable medium, comprising:

a first plurality of instructions for partitioning an integrated circuit into at least one DC-connected component (DCC);

a second plurality of instructions for determining a dominant logic state corresponding to the at least one DCC; and

a third plurality of instructions for calculating a leakage current for the at leas tone DCC corresponding to the dominant logic state.

43. A computer readable medium for analyzing an integrated circuit having a plurality of transistors, each of the plurality of transistors having a first threshold voltage level, comprising:

a first plurality of instructions for calculating a first value based at least in part on delay and leakage corresponding to a second voltage level

for each of the plurality of transistors;

a second plurality of instructions for selecting one of the plurality of transistors based on the first values;

a third plurality of instructions for setting the selected one of the transistors to the second threshold voltage; and

a fourth plurality of instructions for determining a cone of influence of the selected one of the transistors.

44. A computer readable medium, comprising:

a first plurality of instructions for receiving a graph having nodes and edges according to a dominant logic state of an integrated circuit;

a second plurality of instructions for calculating a leakage for each transistor in a first set of transistors;

a third plurality of instructions for modifying the graph based on the first set of transistors; and

a fourth plurality of instructions for calculating a leakage for each transistor in a second set of transistors.